Actions

MICROELECTRONICS Co., Ltd.

Actions-micro AM8269D Datasheet

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Actions Microelectronics Co., Ltd.
701, 7floor, Golder Plaza, No.10 huayuandonglu, Haidian District,
Beijing, China

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Table of Contents

Revision History

Version	Date	Description	Author
1.0	12/24/2018	Initial Create	maweishuo

Terms and Acronyms

Terms and Acronyms	Definition
CF	Compact Flash
SM	Smart Media
XD	xD picture
SD	Secure Digital
Micro SD	Micro Secure Digital
MS	Memory Stick
MS Pro	Memory Stick Pro
MMC	Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
MD	MicroDrive
TF	T Flash
LCD	Liquid Crystal Display
ICE	In-circuit emulation, or in-circuit emulator
JTAG	Joint Test Action Group(ANSI/ICEEE Std.11149.1-1990)
PQFP	Plastic Quad Flat Package
LQFP	Low-Profile Quad Flat Package
BGA	Ball Grid Array
PIP	Picture In Picture
TAP	TEST ACCESS PORT
RGB	Red-Green-Blue color space representation
TCON	Timing controller

General Conventions

Symbol	Description	Notes
Note		
H	In the notes column, an H indicates the pin is hidden behind the actual physical pin listed in the Alternate Functions column and is not included in the pin count. No H indicates the actual pin is listed in the Signal Name column and the Alternate Functions column lists the alternate signals present on the pin.	
Pad GP		
1	Pad group 1	
2	Pad group 2	
Dir/Pol (direction/polarity)		
I	Input	
O	Output	
B	Bidirectional	
Z	Three state output	
Pad Type		
A	Analog pad	
B	Bidirectional	
BS	Bidirectional with Schmitt trigger	
H	High-voltage(up to 3.0 V)tolerant digital input	
I	CMOS input	
IA	Analog input	
IS	Input with Schmitt trigger	
K	Contains an internal weak keeper device	
O	Output	
OA	Analog output	
OD	Open-drain	
PD	Contains an internal pull-down device	
PP[NP]	Can be programmed to non pull, pull down or pull up. The default value is no pull after reset.	
PP[PD]	Can be programmed to non pull, pull down or pull up. The default value is pull down after reset.	
PP[PU]	Can be programmed to non pull, pull down or pull up. The default value is pull up after reset.	
PU	Contains an internal pull-up device	
PWR	power	
Z	High-Z output	
Drive (mA)		
n	Variable drive strength pins.	

1 Introduction

1.1 Overview

The AM8269D processor from Actions-Micro is a highly integrated mix signal SoC target at multi-media applications. The AM8269D emmedded CPU is a high performance, low power 32bit RISC core with DSP instruction extension, which can run as fast as 800MHz.

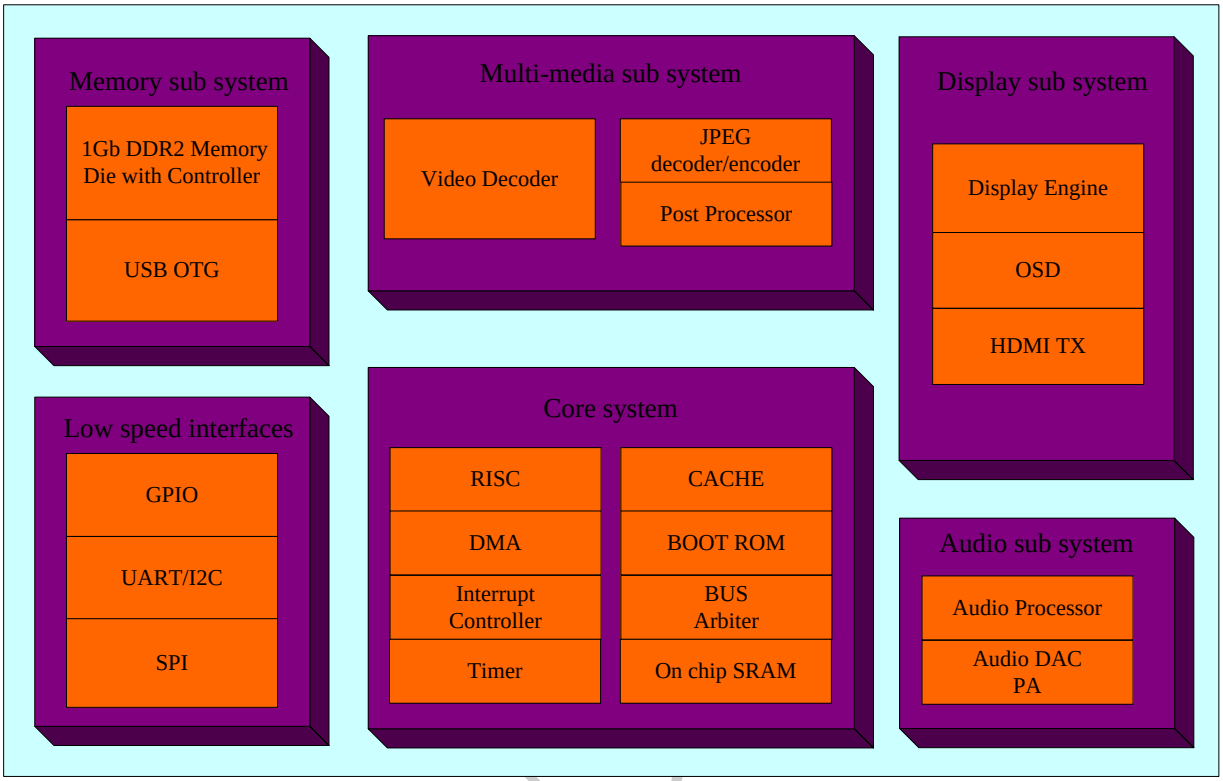
The AM8269D processor features a hardwired multi-format video decoder, which supports a large variety of popular video formats including: H.264, RMVB, MPEG1/2/4 and VC1 at full HD resolution. The AM8269D integrated image/video post processor and display engine provide a powerful image processing ability, such as seamless zoom in/zoom out, cropping, rotation, color space conversion, gamma correction, edge enhancement, dithering, brightness, contrast and saturation adjustment. Moreover, a configurable FIR is reserved for other special effects extension. The 2 layers of OSD window can be configured as large as full screen and the color depth is ranging from 1 bit to 32bit true color.

The AM8269D multi-media processor provided display solutions: with the help of on chip HDMI.

AM8269D is also integrated with 1 USB OTG controllers, UART, I2C, SPI,etc.

There is a 1Gb DDR2 memory die integrated in AM8269D, so no need to hang a DDR2 memory on PCB.

1.2 Block Diagram



AM8269D BLOCK DIAGRAM

2 Feature

The AM8269D provides high level of system integration to support a wide variety of applications. The features of the AM8269D include:

✓ **32BIT RISC CORE**

- 32K byte instruction cache and data cache
- F/W can program from DC up to 800MHz transparently
- DSP instruction for multi-media acceleration
- Static design allows changing clock at run-time for power saving

✓ **VIDEO DECODER**

- Multi-format supported including:

H.264 profile and level	Up to High Profile ,levels 1-4.1
MPEG-4 visual profile and level	Advanced Simple profile(frame picture) , levels 0-5
H.263 profile and level	Profile 0, levels 10-70. Image size up to 720x576, time code extensions not supported
VC-1 profile and level	Simple and Main profile; low, medium and high levels
MPEG-2/MPEG-1	Main profile; low and main levels, MPEG-1 D-picture not support
RV8/9/10	

- 30 frames per second at 1920x1080 resolution for all format
- Adaptive De-interlacing

✓ **JPEG DECODER**

- Support JPEG baseline
- Support YCbCr 4:2:0 planar and semiplanar
- Support YCbYCr & CbYCrY 4:2:2 interleaved
- Support image size: from 80x16 to 4672x3504
- Support rotate: +90° , -90°

✓ **IMAGE/VIDEO POST PROCESSOR**

- Image up/down scaling at arbitrary non-integer scaling ratio
- Separate scaling ratio for horizontal and vertical dimensions
- Image cropping
- Image crossing

- Image rotation, 90 180 and 270 degrees and horizontal/vertical flip
- Image mask, output image writing can be prevented on two rectangular areas
- Support YUV444/YUV422/RGB888/RGB565 for mask window for alpha blending(256 level)
- YUV/RGB conversion
- Maximum output image size up to 1920x1080

✓ **Display Engine**

- YCbCr/RGB conversion, user definable conversion coefficients
- Image up scaling at arbitrary non-integer scaling ratio
- Separate scaling ratio for horizontal and vertical dimensions
- brightness, contrast and saturation adjust
- Edge enhancement
- Dynamic contrast adjust
- Direct mapped Gamma correction for RGB channel separately
- 24bit to 16/18 bit Bayer pattern/1D/2D method dithering
- Support progressive and interlace input format
- Support YUV4:2:2(interleave), YUV4:2:0(semi planar), RGB565, RGB888 input forma
- 16x16 hardware cursor

✓ **OSD**

- Two layers of OSD window with overlap
- 8 level alpha blending for each window
- 1,2,4 or 8 bits OSD bitmap data width
- Transparency pixels allowed in OSD window
- Two configurable OSD palettes
- Each one of the 2 OSD windows can fetch RGB565/ARGB8888 data from system memory directly

✓ **DISPLAY INTERFACE**

- HDMI Tx support, industry standard compliance HDMI 1.2
- Support output size up to 1920x1080
- Configurable horizontal sync interrupt

✓ **AUDIO**

- Multi-format audio decoder:MP1/MP2/MP3/WMA/AAC/AMR-NB/WAV/PCM/ADPCM
- Build in Stereo 18-bit Sigma-Delta DAC: SNR>92db(no a-weight), 18bits,sample rate 8/12/11.05/16/22/24/32/44.1/48
- Support 32 levels volume control

✓ **MEMORY Storage**

- Integrated with a 1Gb DDR2 die which is up to 1066Mbps
- OTP ROM 64bit Chip ID

✓ **DMA CONTROLLER**

- 8 physical channels and 4 bus channels
- Stride mode support
- Software configurable priority

✓ **Boot ROM**

- On chip boot ROM with boot loader
- The system could be loaded from SPI Nor flash

✓ **USB 2.0 OTG**

- Complies with Universal Serial Bus Specification. Revision 2.0.
- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode.
- Supports full-speed or high-speed in peripheral mode.
- Supports USB Mass Storage Class Bulk-Only Transport Revision 1.0 as host or device.
- Supports Electronic still picture imaging Picture Transfer Protocol (PTP)
- Supports direct print function using pict-bridge
- Supports Universal Serial Bus Device Class Definition for Printing Devices Version 1.1 as host
- Supports Universal Serial Bus Still Image Capture Device Definition Revision 1.0 as host
- Configurable/programmable size of endpoints.
- Configurable/programmable single, double, triple or quad buffering.
- Programmable type of endpoints.
- Supports high-speed high-bandwidth Isochronous and Interrupt transfer.
- Supports suspend, resume and power managements function.
- Support USB wakeup

✓ **OTHER INTERFACE**

- UART/I2C/SPI
- 3 external interrupts
- 41 configurable GPIO shared with function pins

✓ **POWER**

- 1.3v for core

- 3.3v/2.5v/1.5v for IO
- Build in 1.5v bandgap reference
- Core PLL, LCD PLL,Audio PLL and DDR PLL support spread spectrum

✓ **PACKAGE**

- QFN 68(epad)

3 Power on Sequence

The power on sequence requirements of the AM7xxx and AM8xxx products are the same, which are shown in the following figure. VDD represents the power pins supplying power for the core. VCC represents the power pins supplying power for the general purpose pads. SVCC represents the power pins supplying power for the DDR2 or DDR3 SDRAM related pads. P_RESETB is the asynchronous reset pin. PWROK is an internal signal. It is low during the power-on phase to reset all the registers in the chip. The system boots at the moment when PWROK turns to high.

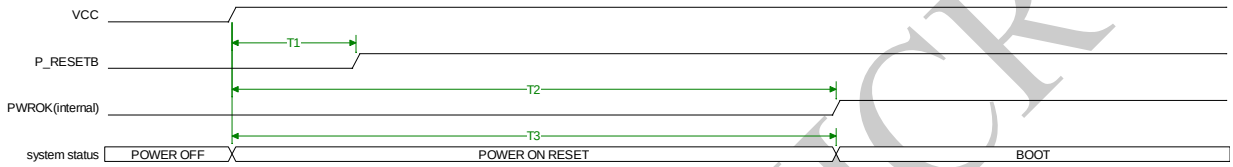


Figure 1 Power on Sequence Diagram

Timing Requirements:

1. $T1 \geq 20ms$
2. $T2 \approx 128ms$
3. $T3$ is equal to the greater one between $T1$ and $T2$
4. The power on sequence of VDD/VCC/SVCC is not cared

4 Registers

Module name	Physical Bass Address	KSEG1 Base Adress
MFP	0x101C0000	0xB01C0000

4.1 Multi-Function PAD Config Registers

4.1.1 MFP Configuration Register-0

Offset=0x0040

Bit	Name	Descriptions						default
		Bit Value	Function	PU/PD	In/Out	Default I	HI/LO	
mfp0[0]	-	-	Reserved					0
mfp0[1]	P_I2CSCL	0	GPIO[1]		B			0
		1	I2C0_SCL	PU2.2K	1/O	1	LOW	0
mfp0[2]	P_I2CSDA	0	GPIO[2]		B			0
		1	I2C0_SDA	PU2.2K	1/O	1	LOW	0
mfp0[3]	P_GPIO0	0	SD_D0		B			0
		1	PWM0		0/1			0
mfp0[4]	P_GPIO1	0	SD_D1		B			0
		1	PWM1		0/1			0
mfp0[5]	P_GPIO2	0	BOOT_SEL 0		1/0			0
		1	SD_D2		B			0
mfp0[6]	P_GPIO3	0	BOOT_SEL 1		1/0			0
		1	SD_D3		B			0
mfp0[7]	P_GPIO4	0	SD_CLK		B			0
		1	I2C1_SCL	PU2.2K	1/O	1	LOW	0
mfp0[8]	P_GPIO5	0	SD_CMD		B			0
		1	I2C1_SDA	PU2.2K	1/O	1	LOW	0
mfp0[10:9]	P_DRVVBUS	0	EJ_DINT	PD100K	1/0			0
		1	DRVVBUS		0/1			0
		10	GPIO[9]		B			0
mfp0[12:11]	P_EXTINT0	0	GPIO[10]		B			0
		1	EXT_INT[0]		1/0	lowact	SP	0
		10	HDMI_HOTPLUG_IN		1/0			0

mfp0[14:13]	P_EXTINT1	0	EJ_TCK	PU100K	1/0	1	LOW	0
		1	GPIO[11]		B			0
		10	EXT_INT[1]	PU100K	1/0	lowact	SP	0
mfp0[15]	P_EXTINT2	0	GPIO[12]		B			0
		1	EXT_INT[2]	PU100K	1/0	lowact	SP	0
mfp0[16]	P_UARTTX	0	GPIO[13]		B			0
		1	UART_TX		0/1			0
mfp0[18:17]	P_UARTRX	0	EJ_TDO		O			0
		1	UART_RX		1/0	1	LOW	0
		10	GPIO[14]		B			0
mfp0[19]	P_TEST	0	(TEST)	PD100K	1/0			0
		1	GPIO[15]		O			0
mfp0[20]	P_SPICLK	0	GPIO[16]		B			0
		1	SPI_CLK		1/O			0
mfp0[21]	P_SPIMOSI	0	GPIO[17]		B			0
		1	SPI_MOSI		1/O			0
mfp0[22]	P_SPIMISO	0	GPIO[18]		B			0
		1	SPI_MISO		1/0			0
mfp0[24:23]	P_SPIHOLD	0	EJ_TMS	PU100K	1/0	1	LOW	0
		1	SPI_HOLD		1/O			0
		10	GPIO[19]		B			0
mfp0[26:25]	P_SPIWP	0	EJ_TRST_N		1/0	1	LOW	0
		1	SPI_WP		1/O			0
		10	GPIO[20]		B			0
mfp0[28:27]	P_SPINSS	0	EJ_TDI	PU100K	1/0	1	LOW	0
		1	GPIO[21]		B			0
		10	SPI_NSS		1/O	1	LOW	0
mfp0[29]	P_SPINSS2	0	GPIO[22]		O			0

5 Pin Out Specification

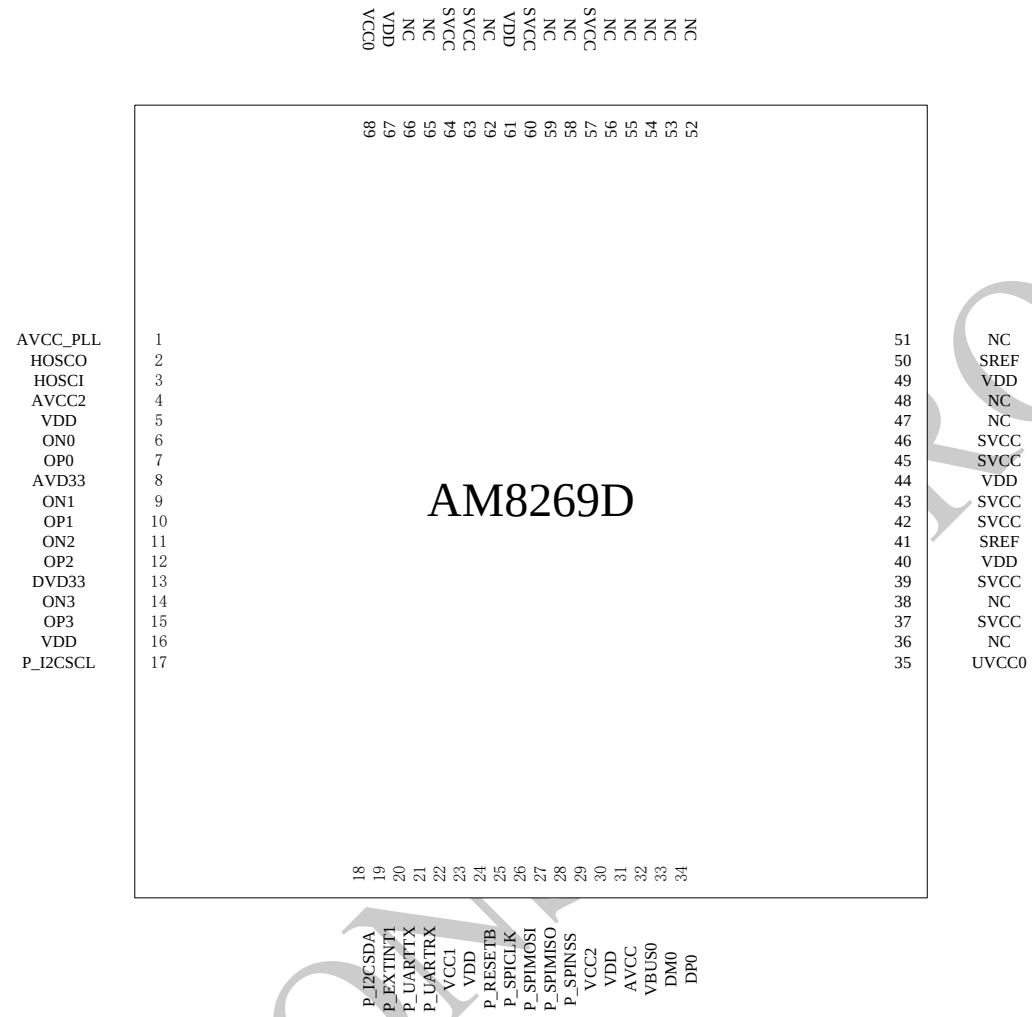
5.1 Pin out table

PINNUM	PIN NAME	TYPE	PIN Function
1	AVCC_PLL	PWR	AVCC_PLL
2	HOSCO	A	HOSCO
3	HOSCI	A	HOSCI

4	AVCC2	PWR	AVCC2
5	VDD	PWR	VDD
6	ON0	A	HDMI
7	OP0	A	HDMI
8	AVD33	PWR	HDMI
9	ON1	A	HDMI
10	OP1	A	HDMI
11	ON2	A	HDMI
12	OP2	A	HDMI
13	DVD33	PWR	HDMI
14	ON3	A	HDMI
15	OP3	A	HDMI
16	VDD	PWR	VDD
17	P_I2CSCL	B	I2CSCL
18	P_I2CSDA	B	I2CSDA
19	P_EXTINT1	B	EXTINT1
20	P_UARTTX	B	UARTTX
21	P_UARTRX	B	UARTRX
22	VCC1	PWR	VCC
23	VDD	PWR	VDD
24	P_RESETB	I	RESETB
25	P_SPICLK	B	SPICLK
26	P_SPIMOSI	B	SPIMOSI
27	P_SPIMISO	B	SPIMISO
28	P_SPINSS	B	SPINSS
29	VCC2	PWR	VCC2
30	VDD	PWR	VDD
31	AVCC	PWR	AVCC
32	VBUS0	A	VBUS0
33	DM0	A	DM0
34	DP0	A	DP0
35	UVCC0	PWR	UVCC0
36	NC	-	-
37	SVCC	PWR	SVCC
38	NC	-	-
39	SVCC	PWR	SVCC
40	VDD	PWR	VDD
41	SREF	PWR	SREF
42	SVCC	PWR	SVCC
43	SVCC	PWR	SVCC
44	VDD	PWR	VDD
45	SVCC	PWR	SVCC

46	SVCC	PWR	SVCC
47	-	-	-
48	-	-	-
49	VDD	PWR	VDD
50	SREF	PWR	SREF
51	NC	-	-
52	NC	-	-
53	NC	-	-
54	NC	-	-
55	NC	-	-
56	NC	-	-
57	SVCC	PWR	SVCC
58	NC	-	-
59	NC	-	-
60	SVCC	PWR	SVCC
61	VDD	PWR	VDD
62	NC	-	-
63	SVCC	PWR	SVCC
64	SVCC	PWR	SVCC
65	NC	-	-
66	NC	-	-
67	VDD	PWR	VDD
68	VCC0	PWR	VCC0

5.2 Pin out diagram



AM8269D PIN-OUT DIAGRAM

6 Operating Conditions

Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply (3.3V)	3.8	V
Vsvcc	Power Supply (1.5V)	1.575	V
V_{dd}	Power Supply (1.35V)	1.4	V
V_{IN}	Input Voltage	-0.5~4.6	V
V_{OUT}	Output Voltage	-0.5~4.6	V
T_{STG}	Storage Temperature	0~75	℃
Tc	Operation Temperature (Case Surface)	0~90	℃
Ta	Ambient Temperature	0~60	℃

Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply (3.3V)	3.0	3.3	3.6	V
Vsvcc	Power Supply (1.5V)	1.425	1.5	1.575	V
V_{dd}	Power Supply (1.35V)	1.3	1.35	1.4	V
T_a	Ambient Temperature	0	35	60	℃

DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and V_{CC} = 3.0V~3.6V, T_j = 0 to +70) ℃ ℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.2			V
V_{T-}	Schmitt Input Low Voltage				0.9	V
V_{T+}	Schmitt Input High Voltage		1.9			V
V_{OL}	Output Low Voltage	4mA			0.4	V
V_{OH}	Output High Voltage	4mA	2.4			V

7 Crystal Requirements

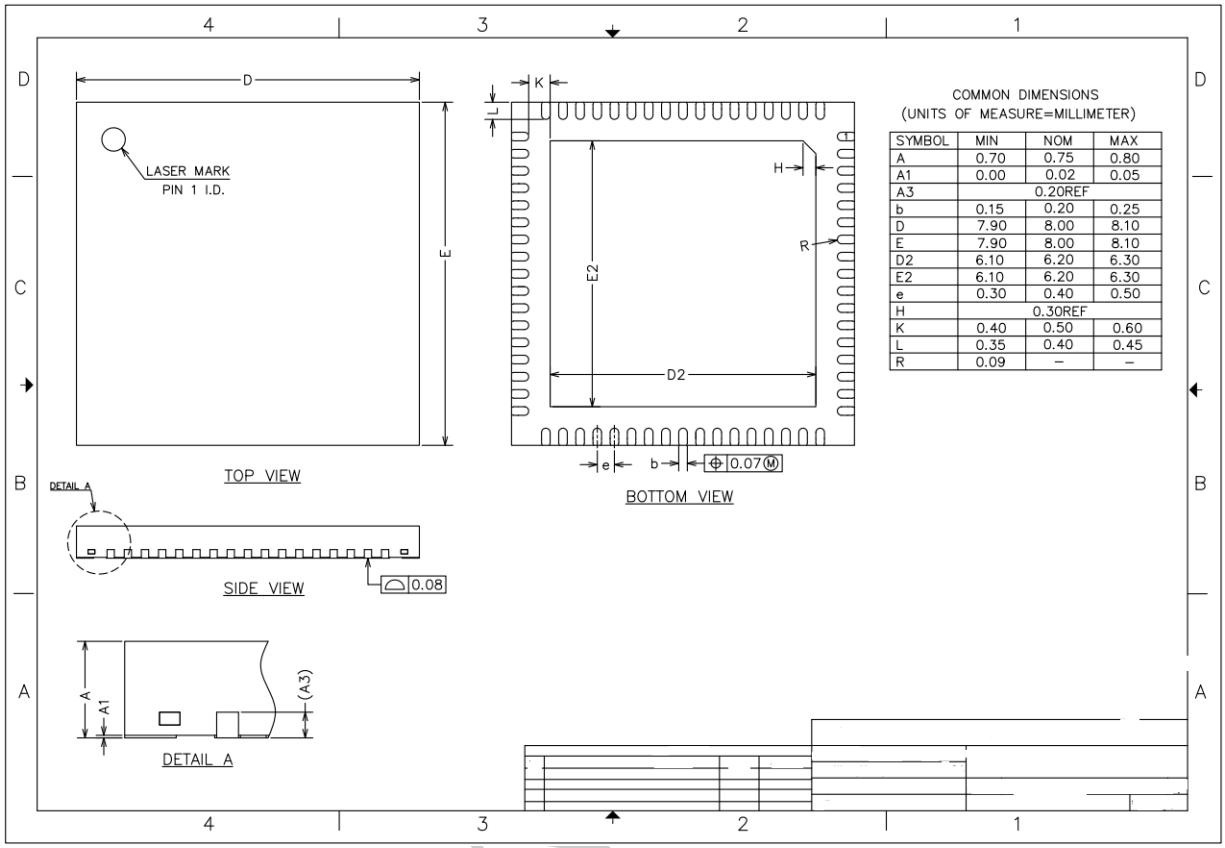
Requirements for 24MHz oscillator.

Description	Specification Requirement
Nominal Frequency	24MHz
Oscillation Mode	Fundamental
Frequency Tolerance at 25℃	±30ppm
Temperature Stability	±50ppm
Shunt Capacitance (Co)	7pF（max）
Load Capacitance (CL)	12pF~18pF
Equivalent Series Resistance (ESR)	50ohm（max）
Drive Level	500uW （max）
Aging (at 25℃)	±3ppm/year
Insulation Resistance	10meg
Net Weight	This will be various. No limitation.
Operating Temperature Range	-10~90℃
Storage Temperature Range	-45~125℃

Requirements for 32.768KHz oscillator.

Description	Specification Requirement
Nominal Frequency	32.768KHz
Oscillation Mode	Fundamental
Frequency Tolerance at 25℃	±30ppm
Temperature Stability	±50ppm
Shunt Capacitance (Co)	7pF（max）
Load Capacitance (CL)	12pF~18pF
Equivalent Series Resistance (ESR)	50ohm（max）
Drive Level	500uW （max）
Aging (at 25℃)	±3ppm/year
Insulation Resistance	10meg
Net Weight	This will be various. No limitation.
Operating Temperature Range	-10~90℃
Storage Temperature Range	-45~125℃

8 Mechanical Specification



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.10	6.20	6.30
E2	6.10	6.20	6.30
e	0.30	0.40	0.50
H		0.30REF	
K	0.40	0.50	0.60
L	0.35	0.40	0.45
R	0.09	–	–